ZUKIL

PERSONAL COMPUTER
BUS STANDARD
P996

Draft D2.02

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P996 Working Group
of the Microprocessor Standards Committee

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Preliminary - Subject to Change

Abstract

This standard is a specification of an 8 and 16 bit personal computer backplane bus. It is based on the PC and AT buses originally developed by IBM and widely used throughout the personal computer industry. There are 88 active signals and 10 power and ground lines contained in two PCB edge connectors (62 and 36 pins). Two form factors are specified, 3.9 inches x 13 inches with one connector for 8 bit adapters and 4.5 inches x 13 inches with two connectors for 16 bit adapters.

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Preface

This Preface is not part of the 996 bus specification.

This document represents the current status of the work of the P996 committee.

Appendices to this document should be considered as options, not as part of the standard. However, they do generally conform to the electrical and mechanical specifications described in this document.

Related documents include:

PCET Hardware Subcommittee Bus Proposal, Document 0886-006A, revision level 1.0, 2 October 1986.

IBM PC/AT Hardware Technical Reference 6183355, Revised Edition, March 1986, IBM Corporation

IBM RT/PC Hardware Technical Reference 6489893, First Edition, November 1985, IBM Corporation

ISA Bus Specification and Application Notes, revision 2.01, Sept 12, 1989, Intel Corporation

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t originated in 1986 in the efforts of the **PCET**, which was a PC industry group formed to codify and extend the **PC/AT** I/O channel and became an IEEE working group in 1987. A PAR was issued, P996, and two subcommittees were formed, one to extend the capabilities of the bus and the other to codify the existing defacto industry tandard bus.

The 8 bit I/O channel found in the IBM **PC** and **XT** and later extended to 16 bits in the **AT**, has become a defacto standard found in millions of IBM and IBM-compatible personal computers. However, because no detailed timing pecifications were released by IBM there always has been confusion as to what constituted "compatibility" to the PC and **AT** buses.

- Board designers had to test their products in many different PC and AT systems to establish some degree of confidence that they would work correctly when installed in user's systems.
- System designers had to test many different boards in their systems and compare timing and circuits to other widely used PCs and ATs as well as the original IBM designs.

n all above cases this just guaranteed compatibility to a "typical" system since a "worst case" system did not normally exist. The "reference" was an 8MHz IBM model 339 **PC/AT** with worst case timing numbers specified.

This document is intended to define the operation of the **PC/AT** I/O channel as *concisely* as possible for both ystem and add-in board designers and manufacturers.

Revision History

Draft 2.02 13 July 1990

1. Clarify definition of Temporary Master in section 1.3.5.2.
2. Correct source of refresh address described in section 3.6.
3. Correct/clarify **AEN** operation during Alternate Master operations A Alternate Master is permitted to perform I/O operations. in section 3.4.
4. Correct bracket width dimension in Figure 8.3. The total width of the bracket is 0.850 including the jog. not 0.950.

Draft 2.01 14 May 1990

1. Addition of a statement in Section 2.5.1, "Data Transfer Operations"describing under what circumstances the 11ηS bus settling time is included.
2. Description for parameter 16 changed from "Command" to "Read Command" in Table 3.1 on page 3.3.
3. Parameters 20a changed from 70/159 to 81/103 and 20b changed from 373/462 to 384/406 in Table 3.1 on page 3.3.
4. Parameters 25a and 25b description changed from "Data setup to **IOCHRDY** deasserted" to "Data setup to **IOCHRDY** asserted" and values from 85/74 to -74/-85 and 75/64 to -64/-75, respectively, in Table 3.1 on page 3.3.
5. Correct front of card to front of edge connector tab dimension from 0.705 to 0.905 and bracket to front of edge connector tab from 0.740 to 0.940 in Figure 8.2 on page 8.5 and Figure 8.1 on page 8.4.
6. Note for Table A.1 on page A.5 changed to indicate that the pullups have a value of 4K7Ω.

D2.00 18 January 1990

1. Delete T14, T33, T38 from Memory and I/O Timing table.
2. T36, T37 changed from min to max.
3. T1 numbers referenced from front to back edge of **BALE**.
4. T7 c,d values folded into T7 a,b respectively.
5. T34, Change description from SD enabled to SD disabled.
6. T17, remove 8b from size column, Endxfr is only defined for 16b memory.
7. T8c, remove IO and 8b from type and size columns. Endxfr is defined only for 16b memory. Change description from 0WS to Endxfr.
8. T8d, remove 16b from size column to correspond to description.
9. Add values for T28-37
10. T16 added to DMA timing table.
11. Driver Table, < 1M should be on **SMEMR***, not **MEMR***, etc.

D1.90 11 December 1989

1. Add text descriptions of Permanent Master driven signals in DMA section.
2. Add comment about skirts on XT and AT form factors
3. Delete T27 from the memory and I/O timing table since T28 and T29 qualify **ENDXFR***.
4. Add T5b **MEMCS16*** deasserted from **LA<23..17>**
5. Add T9 **SA<19..00>** setup to **BALE** deasserted
6. Add T11d, 8b write setup, odd address
7. Add T13c, 8/16b I/O command off
8. Add T15c, 8b memory write data hold
9. Add T30-32, T34-38 to the memory and I/O timing table.
10. Change reference point for T1 from front to back edge of **BALE**.
11. Change T1, 2, 3, 4, 5, 7, 8, 10, 11, 12, 13, 17
12. Compact Revision History

D1.80 14 November 1989

1. Definition of **SYSCLK** upper frequency in Signal Definition/Utilities/Controls from 8.00 to 8.33MHz

D1.77 25 September 1989

1. Table 3.3, DMA timing, 3b change driver/receiver mins from 30/19 to 0/0.
2. Change reference number 2 in figure 3.6 from **SA<16..0>** to **IOR*,MEMR***, to **MEMR*, IOW*, IOR***.
3. Correction of **OSC** frequency in Signal Definition/Utilities/Controls from 14.3818 to 14.31818MHz.
4. Definition of **SYSCLK** lower frequency in Signal Definition/Utilities/Controls from 4.77 to 6MHz
5. Add note to Signal Definition/Utilities/Commands stating that **SMEMx*** will be driven by the Permanent Master if **MEMx*** is driven by an Alternate Master
6. Change TM column in Table 8.11 Driver Requirements from "D/R" to "D".
7. Revised Figures 8.1 and 8.2 showing 8 and 16 bit card dimensions.
8. Merged Figures 8.3 and 8.4 containing bracket dimensions and card/bracket alignment.
9. Cross References changed from page to section numbers.
10. Changed voltage tolerances for boards and backplanes to +5,-2.5% for +5V and +5,-5% for all other power supplies.
11. Ioh changed from -0.4 to -3.0mA for 24mA drivers.
12. Iol changed for **TC** from 8 to 2.0mA.
13. Iol changed for **DACK** from 8 to 3.2mA.
14. **DACK** and **TC** are restricted to driving only one load per adapter.
15. Revise Refresh timing numbers, add **AEN** waveform to refresh waveform figure.

D1.76 9 August 1989

1. Added **ENDXFR*** timing relative to **SYSCLK** and **ENDXFR*** minimum pulse width.

2. Changed capacitive loading for boards from 20 to 15pF.

D1.75 18 July 1989

1. Reversed order of Pin Assignment tables to conform to view from top of motherboard from the front.

D1.74 10 July 1989

1. Changed timing tables and figures to agree with PC/96. Driver column not specified in Timing Tables because electrical characteristics of the bus are implementation specific.

D1.71 26 January 1989

D1.70 9 January 1989

- Change signal names to conform to IEEE conventions - "*" following the name.
- Change name to Personal Computer Bus Standard

D1.60	***4 October 1987***
D1.51	***17 September 1987***
D1.50	***12 August 1987***
D1.42	***11 August 1987***
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D1.40	***20 May 1987***
D1.33	***28 April 1987***
D1.32	***1 April 1987***
D1.2	***24 March 1987***
D1.1	***17 February 1987***
D1.0	***20 January 1987***

1. Introduction

This document is intended to provide a common specification for the development of systems and adapter boards that operate in that system using the P996 Bus. It is the intent of the P996 committee to develop an industry standard definition that allows system and adapter board developers, system integrators and end users confidence in compatibility of products designed to meet the P996 specification.

The intent of this specification is to allow for the use of most PC and PC/AT adapter cards in conjunction with P996. P996 allows for higher performance than those buses but allows users to take advantage of existing adapter cards. It can also be used as a specification for the operation of the 8 bit I/O channel found in PC and PC/XT systems.

1.1 Specification Objectives

The P996 bus specification defines the interface for the use of interconnecting data storage, data processing, and peripheral control devices in a closely coupled configuration.

This specification describes physical, electrical characteristics and protocol of the P996 bus.

1.2 System Elements

1.2.1 Physical Structure

The physical structure of the P996 bus defines the relationship of the adapter connectors to the required size for adapters attempting to meet the standard. Two different adapter form factors have been identified that would conform to the P996 bus structure:

- 8 bit form factor card adapter (PC height) physically compatible to the PC/XT.
- 16 bit form factor card adapter (AT height) physically compatible to the PC/AT

1.2.2 Functional Structure

The functional structure of the P996 bus consists of four groups of signal lines called busses. These signal groups are intended for the following functions:

- Data Transfer
  - Address
  - Data
- Utilities
  - Controls
  - Commands
  - Transfer Response
- Bus Arbitration
- Interrupts

Each of those functions are discussed in in detail in Section 1.3.5.3, "Signal Definition" of this document.

1.3 Specification Terminology

1.3.1 Bit Numbering Conventions

The busses of the P996 bus specification are numbered from '0' (a single digit), appended to the name, for least significant bit to the appropriate number for the most significant element in the bus. The one exception is the **LA** bus that is numbered to represent the address value that it carries. For the P996 busses the following are the least and most significant bits:

Most	Significant	Least
LA23	———	LA17
SA19	———	SA0
D15	———	D0

1.3.2 Byte Numbering Conventions

Sixteen bit words are addressed on an even byte address boundary (A0=0). The following table shows the alignment in memory of byte and word addresses.

15 08	07 00	byte address
—— word<6>——		6
—— word<4>——		4
byte<3>	byte<2>	2
byte<1>	byte<0>	0

1.3.3 Signal Line States

A signal line is always assumed to be in one of two levels or in transition between these levels. The term LOW refers to a voltage less than or equal to V*il* (0.8V) with respect to the ground reference provided at the bus connector. The term HIGH refers to a voltage equal to or greater than V*ih* (2.0V) with respect to the same reference. These voltage levels are defined in Table 8.2 on page 8.1 and Table 8.3 on page 8.1

1.3.4 Active Polarity

Signal names carry information as to the logic level of the asserted state. A signal name with a "*" following it is active (asserted) when it is LOW. A signal name with no trailing "*" is active (asserted) when it is HIGH.

1.3.5 Terminology

1.3.5.1 General

Backplane: A circuit board with one or more bus connectors which provides signals for communications between bus adapters.

Bus Adapter: Any device which occupies a bus slot and responds to or generates Memory or I/O addresses, generates interrupts or in any way communicates with other elements (Permanent Master or bus adapters) using the system bus is considered a bus adapter.

Bus: A set of signal lines to which a number of devices are connected and over which information is transferred between them.

Byte: A set of 8 signals or bits taken as a unit.

KBytes (K): 'KBytes' refers to 1,024 bytes.

MBytes (M): 'MBytes' refers to 1,048,576 bytes.

Slot: is a physical location on the bus that allows connection of bus adapters to the backplane.

Word: A set of 16 signals or bits taken as a unit. A word is composed of two sequentially addressed bytes.

1.3.5.2 Protocol

Alternate Master: is any device that can take control of the bus through assertion of the `MASTER*` signal. It has the ability to generate addresses and bus control signals in order to perform bus operations. All Alternate Masters must be 16 bit devices and drive SBHE*.

Bus Exchange: The process by which the bus mastership is passed between different adapters on the bus. This process is defined in Section 3.4, "Alternate Master Operations". The exchange is designed in such a way as to allow reliable system operation with multiple bus masters.

Bus Ownership: The Current Master possesses bus ownership and can assert any bus control, address and data lines.

Current Master: The Permanent Master, Temporary Master or Alternate Master which currently has ownership of the bus.

Initiator: is any device which generates addresses and strobes according to the defined protocol of the bus to cause a transfer of information to occur on the bus. The initiator is characterized by the generation of address and control lines rather than responding to those signals. A Bus Adapter can be an initiator, target or both.

DMA transfer: is initiated by asserting DMA request. The transfer is controlled by the Current Master.

DMA device: is defined as any device which generates a DMA request but requires that the permanent bus masters' logic support the actual transfer of data and gating on the bus.

Permanent Master: Each P996 bus will have a device known as the Permanent Master that provides certain signals and bus control functions as described in Section 3.5, "Permanent Master". The Permanent Master function can reside on a Bus Adapter or on the backplane itself.

Target: is any device that responds to an address and control inputs on the bus to perform I/O, memory or control functions. The target is characterized by the receiving of address and control signals to accomplish a bus operation.

Temporary Master: A Temporary Master is defined as a device that is capable of generating a DMA request to obtain control of the bus and responding to an acknowledge signal in conjunction with an I/O read or write. The Permanent Master's DMA control logic coordinates a simultaneous memory access and I/O operation based on this request. Addresses, memory and I/O control are generated by the DMA device on the Permanent Master.

1.3.5.3 Electrical

Open-Collector: A bus signal connection that can be driven to a logic '0' level only. A pullup resistor to the positive supply is required to establish a logic '1' level. It can also be implemented with a tri-state driver by controlling the output enable and forcing the input. Drive capability for P996 open-collector signals is defined in Table 8.4 on page 8.3.

Totem-Pole: is a bus signal connection that is capable of driving the bus to the logic '1' or logic '0' level. It cannot be disabled. Drive capability for P996 totem-pole signals is defined in Table 8.4 on page 8.3.

Tri-state: is a bus signal connection that presents low leakage current on the bus in the disabled state. This signal is capable of driving the bus to either the logic '1' level or logic '0' level when enabled. Drive capability for P996 tri-state signals is defined in Table 8.4 on page 8.3.

2. Signal Definition

2.1 *Introduction*

This section defines each signal and its function. Detailed information of sequences are described in Section 2.5.1. "Data Transfer Operations".

2.2 *Data Transfer*

2.2.1 Address

The address bus consists of two sections, the first is the pipelined or un-latched address which is valid only with respect to the `BALE` strobe. The address for the next access can become available on the `LA23..LA17` lines before the end of the current cycle. The balance of the addresses are defined to be stable throughout the bus cycle.

LA23..LA17: The address signals `LA23..LA17` define the selection of a 128KB section of memory space within the 16MB address range of the sixteen bit data bus. These signals are *Active HI*. The validity of the `MEMCS16*` depends on these signals only. These address lines are presented to the system with tri-state drivers. The Permanent Master drives these lines except when a Alternate Master cycle occurs, when the Temporary Master drives these lines. The `LA` signals are not defined for I/O accesses.

SA19..SA0: The address signals `SA19..SA0` define the selection with the granularity of one byte within the 1MB section of memory defined by the `LA` address lines. The address lines `SA19..SA17` that are coincident with `LA19..LA17` are defined to have the same value as `LA19..LA17` for all memory cycles. These signals are *Active HI*. These address lines are presented to the system with tri-state drivers. The Permanent Master drives these lines except when a Alternate Master cycle occurs when the Temporary Master drives these lines. During a refresh initiated transfer only `SA7..SA0` are valid.

SBHE*: is an *Active LO* signal that indicates that a byte is being transferred on the upper byte (`SD15..SD8`) of the sixteen bit bus. All bus masters will drive this line with a tri-state driver.

2.2.2 Data

The data bus is the primary vehicle for the exchange of information within the P996 structure. These busses can be driven by either a Initiator or a Target in a particular bus transfer. The signals are *Active HI*, tri-state signals.

SD15..SD8: are defined for the high order byte of a sixteen bit bus. Memory or I/O transfers on this bus are defined when `SBHE*` is active.

SD7..SD0: are defined for the low order byte of a sixteen bit bus and the only bus for eight bit adapters and systems. Memory or I/O transfers on this bus are defined for 8 bit operations with even or odd addresses and for 16 bit operations for odd addresses only. The signals `SA0` and `SBHE` are used to define the data present on this bus. Byte multiplexing is described in Section 3.3, "DMA Operations".

SBHE*	SA0	SD15..SD8	SD7..SD0	Comments
0	0	Odd	Even	Word transfer
0	1	Odd	Odd	Byte transfer on SD15..SD8.
1	0	-	Even	Byte transfer on SD7..SD0.
1	1	-	Odd	

Table 2.1. Data Alignment with 16 bit Bus Adapter

2.3 *Utilities*

2.3.1 Controls

SYSCLK: This clock signal may vary in frequency from 6MHz to 8.33MHz, however, timing parameters shall not be referenced to this clock.

OSC: This is a clock signal with a 14.31818 MHz ±50ppm frequency and a 50±5% duty cycle. This signal is driven by the Permanent Master.

RESETDRV: This *Active HI* signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted on the bus a specified minimum amount of time to insure the adapters in a system are properly reset. When active all adapters should turn off or tri-state all drivers connected to the I/O channel. This signal is driven by the Permanent Master.

2.3.2 Commands

The following signals are used to control data transfer operations on the P996 bus.

BALE: is an *Active HI* signal is used to latch valid addresses from the current Bus Master on the falling edge of `BALE`. During DMA, refresh and Alternate Master cycles, `BALE` is forced HIGH for the duration of the transfer. `BALE` is driven by the Permanent Master with a totem-pole driver.

IOR*: is an *Active LO* signal driven by the Current Master to indicate a I/O read operation. I/O mapped devices using this strobe should decode for selection of adapter and address based on `SA15..SA0` and `AEN`. Additionally, DMA devices will use `I/OR*` in conjunction with the appropriate `DACK`*n*`*` to decode a DMA transfer from the I/O device. The Current Master will drive this line with a tri-state driver. The Permanent Master also ties this line to `+5V` through a 4.7KΩ resistor to insure the signal is inactive during the exchange of bus masters.

IOW*: is an *Active LO* signal driven by the Current Master to indicate a I/O write operation. I/O mapped devices using this strobe should decode for selection of adapter and address based on `SA15..SA0` and `AEN`. Additionally DMA devices will use `-IOW` in conjunction with the appropriate `DACK`*n*`*` to decode a DMA transfer from the I/O device. The Current Master will drive this line with a tri-state driver. The Permanent Master also ties this line to +5V through a 4.7KΩ resistor to ensure that it is inactive during the exchange of bus masters.

SMEMR*: is an *Active LO* signal driven by the Permanent Master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses `SA19..SA0` only. All bus masters will drive this line with a tri-state driver. The Permanent Master also ties this line to +5V through a 4.7KΩ resistor to ensure that it is inactive during the exchange of bus masters.

SMEMW*: is an *Active LO* signal driven by the Permanent Master to indicate a memory write operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses `SA19..SA0` only. All bus masters will drive this line with a tri-state driver. The Permanent Master also ties this line to +5V through a 4.7KΩ resistor to ensure that it is inactive during the exchange of bus masters. If an Alternate Master drives `MEMW*`, the Permanent Master will drive `SMEMW*` delayed by an internal multiplexer.

MEMR*: is an *Active LO* signal driven by the Current Master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses `LA23..LA17` and `SA19..SA0`. All bus masters will drive this line with a tri-state driver. The Permanent Master also ties this line to +5V through a 4.7KΩ resistor to ensure that it is inactive during the exchange of bus masters.

MEMW*: is an *Active LO* signal driven by the Current Master to indicate a memory write operation. Memory mapped devices using this strobe decode addresses `LA23..LA17` and `SA19..SA0`. All bus masters will drive this line with a tri-state driver. The Permanent Master also ties this line to +5V through a 4.7KΩ resistor to ensure that it is inactive during the exchange of bus masters.

Note: If an Alternate Master drives `MEMx*`, the Permanent Master will drive `SMEMx*` delayed by an internal multiplexer.

2.3.3 Transfer Response

IOCS16*: is an *Active LO* signal driven by an I/O-mapped adapter indicating that the I/O device located at the address on the bus is sixteen bits wide. This open collector signal with a 300Ω pullup is driven based only on `SA15..SA0` (not `IOR*` or `IOW*`) when `AEN` is not asserted.

MEMCS16*: This *Active LO* signal is driven by a memory-mapped adapter indicating that the memory device located at the address on the bus is sixteen bits wide. This open collector signal with a 300Ω pullup is driven based on `LA23..LA17` only.

ENDXFR*: is an *Active LO* signal asserted by an 16 bit memory mapped device that may cause an early termination of the current transfer. It should be gated with `MEMR*` or `MEMW*` and is not valid during DMA transfers. `IOCHRDY` has precedence over `ENDXFR*`. It is called `OWS*` on some implementations. This is an open collector signal with a 300Ω pullup.

IOCHRDY: is an *Active HI* signal driven inactive by the target of either a memory or I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. `IOCHRDY` has precedence over `ENDXFR*`.

IOCHCK*: is an *Active LO* signal driven active by an adapter detecting a fatal error during bus operation. This open collector signal is driven LOW typically causing a non-maskable interrupt.

2.4 Bus Arbitration

2.4.1 DMA

DRQ0..DRQ3,DRQ5..DRQ7: are *Active HI* signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. `DRQ1..DRQ3` request 8 bit DMA operations while `DRQ5..DRQ7` request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The Permanent Master monitors this signal to determine which if any of the DMA devices are requesting the bus.

These lines are not guaranteed unless a bus adapter has been configured into the system that drives this line specifically. Therefore, it is the responsibility of the Permanent Master to 'mask' request inputs through software.

DACK0*..DACK3*,DACK5*..DACK7*: are *Active LO* signals driven by the Permanent Master to indicate that a DMA operation can begin. They are driven with a totem pole driver at all times for those DMA channels that are attached.

AEN: is an *Active HI* totem-pole signal driven by the Permanent Master to indicate that the address lines are driven by a DMA controller. The assertion of `AEN` disables response to I/O port addresses when the I/O command strobes are asserted. When `AEN` is asserted only the device asserting `DRQ`*n* should respond.

REFRESH*: is an *Active LO* signal driven by the Current Master to indicate a memory refresh operation. The Current Master will drive this line with a tri-state driver.

TC: This *Active HI* signal is asserted during a read or write command indicating that the DMA controller has reached a terminal count for the current transfer. `DACK*`*n* must be presented by the bus adapter to validate the **TC** signal.

2.4.2 Arbitration Control

MASTER*: is an *Active LO* signal driven by a DMA bus adapter to indicate that the adapter is going to perform an Alternate Master cycle after accomplishing a bus exchange. This open collector signal is driven only when the DMA adapter has received the DMA acknowledge assigned in the system by configuration.

2.5 *Interrupts*

2.5.1 Requests

IRQ3..IRQ7, IRQ9..IRQ12, IRQ14..IRQ15: are *Active HI* open collector signals which indicate the presence of an interrupting bus adapter. `IRQ3..IRQ7` and `IRQ9` are available on the `P1` (8 bit) connector while `IRQ10..IRQ12` and `IR14..IRQ15` are available on the `P2` (16 bit) connector providing a total of eleven interrupts for a system. Because of the use of pullups, unused interrupt inputs must be masked.

Additional interrupts within a system can be accomplished through the use of shared interrupts as described in Section 4.2, "Shared Interrupts". It should be noted that the shared interrupt concept requires that the interrupting adapter on the bus indicates the need for interrupt service with a pulse rather than a level. The hardware supporting the interrupt arbitration must be designed (or programmed) to be edge rather than level sensitive.

3. Data Transfer Operations

3.1 *Introduction*

The sequence and the timing of the defined bus data transfer, interrupt, DMA and Alternate Master and other event sequences are shown with an explanation of the dependencies. Section 3.2, "Memory and I/O Operations" specifies memory and I/O operations for standard non-DMA transfers when

`((AEN = L) OR (MASTER* = H)) AND (REFRESH* = H)`

DMA sequences are defined showing the aspects of the sequences that are unique to DMA transfers. The transfers defined for the Permanent Master also apply to DMA devices with the indicated limitations. Section 3.3, "DMA Operations" specifies cycle operations for DMA transfers when

`(AEN = H) AND (REFRESH* = H)`

Section 3.6, "Refresh" specifies refresh operations when `REFRESH*` is asserted.

Each section consists of a timing specification table followed by one or more timing figures.

3.2 *Memory and I/O Operations*

Table 3.1 on page 3.3 is a summary of memory and I/O operation timing. Many of the parameters are used for several of the timing diagrams describing the various transfer operations on the bus. Figure 3.1 on page 3.4 thru Figure 3.3 on page 3.6 describe the timing sequences for 8 and 16 bit memory and I/O transfers on the bus. 8 and 16 bit memory and I/O extended timing (using `IOCHRDY`) transfers are shown in Figure 3.4 on page 3.7 and 16 bit memory compressed (using `ENDXFR*`) transfers are shown in Figure 3.5 on page 3.7.

3.2.1 Memory Read Default Timing

The start of a cycle is indicated by the `LA23..LA17` address lines being driven and `BALE` going active. The addressed device decodes the `LA23..LA17` address lines and drives `MEMCS16*` to indicate that the device is capable or not capable of 16 bit transfers. On the falling edge of `BALE`, the remaining address lines `SA19..SA0` become valid. The falling edge of `MEMR*` or `SMEMR*` indicate that the cycle is to be a memory read cycle, the read data is then placed on the bus by the target device and is read on the rising edge of `MEMR*` or `SMEMR*`.

3.2.2 Memory Read Extended Timing

For extended timing, the `MEMR*` and `SMEMR*` strobe widths are extended to allow more time for the read data to become available. After `MEMR*` and `SMEMR*` become active, the target drives `IOCHRDY` inactive until the read data becomes available at which time `IOCHRDY` goes active and the cycle completes as it did in the default timing case.

3.2.3 Memory Read Compressed Timing

For compressed read timing, the `MEMR*` and `SMEMR*` strobe widths can be shortened by asserting `ENDXFR*` when a valid memory address qualified with `MEMR*` has been recognized and the requested data has been placed on the `SD` bus. The Current Master is then free to immediately deassert `MEMR*` and `SMEMR*` as soon afterwards as is convenient (the data has been guaranteed latched). The target being read is responsible for ensuring sufficient data hold time for the initiator to latch the data by not removing the data from the `SD` bus until `MEMR*` has been deasserted. This type of read timing is valid only for 16 bit memory operations.

3.2.4 Memory Write Default Timing

The start of a memory write cycle is very similar to a memory read cycle. The `LA23..LA17` address lines become valid and `BALE` goes active, the addressed device decodes the `LA23..LA17` address lines and drives `MEMCS16*` to indicate that the device is capable or not capable of 16 bit transfers. On the falling edge of `BALE`, the remaining address lines `SA19..SA0` become valid. A memory write cycle is indicated by the leading edge of `MEMW*` or `SMEMW*`. The write data is available on the `SD7..SD0` lines (or `SD15..SD0` lines for 16 bit transfers) prior to

`MEMW*` and `SMEMW*` going active and remains valid until after the trailing edges of `MEMW*` and `SMEMW*`. This allows the write data to be latched on either edge of `MEMW*` and `SMEMW*`.

3.2.5 Memory Write Extended Timing

Extended write timing is similar to the memory read case, in that the `MEMW*` and `SMEMW*` are widened to allow more time for the target device to latch the write data on the **SD** lines. After `MEMW*` and `SMEMW*` become active, the target drives `IOCHRDY` inactive which will hold `MEMW*` and `SMEMW*` active until `IOCHRDY` is released.

3.2.6 Memory Write Compressed Timing

For compressed write timing, the `MEMW*` and `SMEMW*` strobe widths can be shortened by asserting `ENDXFR*` when a valid memory address qualified with `MEMW*` has been recognized and the requested data has been latched from the **SD** bus. The Current Master is then free to immediately deassert `MEMW*` and `SMEMW*`. The target being written is responsible for ensuring sufficient data hold time to latch the data either by waiting to assert `ENDXFR*` until the data is latched or by providing sufficient path delays in its logic. This type of write timing is valid only for 16 bit memory operations.

3.2.7 Bus Settling Factor

The inclusion of a factor for bus settling will insure a high degree of compatibility between systems incorporating the P996 bus. It assumes a fully loaded 8 slot backplane, additional slots will require a longer settling time.

A bus settling time of 11ηS is sufficient to account for backplane impedance, trace length and load violations, driver type, and relative slot location of driver and receiver.

For a low to high transition, the time is measured from V*ol* (0.5V) at the driver to V*ih* (2.0V) at the receiver. For a high to low transition, the time is measured from V*oh* (2.4V) at the driver to V*il* (0.8V) at the receiver.

This settling time appears in several ways in the timing tables as a difference between the delay times at the driver and receiver:

- Two signals generated by drivers on the same device. The skew of their arrival at receivers on another device can be a maximum of 11ηS.
- From a driver on one device to a receiver on another and return from a driver on the other to a receiver on the first device. The total round trip is 22ηS.
- Rise time for a line driven by an open-collector driver terminated with a pull-up resistor. The settling time for these entries is 22ηS and 78ηS for 300Ω and 1KΩ pull-up resistors, respectively, for a single direction of travel.

ref	Type	Size	Description	Driver		Receiver	
				Min	Max	Min	Max
1	M,IO	8/16	LA setup to BALE deasserted	111		100	
2	M,IO	8/16	BALE pulse width	61		50	
3	M,IO	8/16	LA hold from BALE deasserted	26		15	
4a	M	16	LA setup to MEMx* asserted.	120		109	
b	M	8	LA setup to MEMx* asserted.	183		172	
5	M	8/16	MEMCS16* valid from LA		66		102
6	M	8/16	MEMCS16* hold from LA	0		0	
7a	M	16	SA,SBHE* setup to MEMx*	39		28	
b	IO	16	SA,SBHE* setup to IOx*	102		91	
c	M,IO	8	SA,SBHE* setup to IOx* or MEMx*	102		91	
8a	M	16	Command width	240		219	
b	IO	16	Command width	165		154	
c	M	16	Command width with ENDXFR* asserted	103		92	
d	M,IO	8	Command width (Note 1.)	541		530	
10a	M	16	Read data access		173		195
b	IO	16	Read data access		110		132
c	M,IO	16	Read data access with ENDXFR* asserted.		48		70
d	M,IO	8	Read data access (Note 2.)		482		504
11a	M	16	Write data setup	-34		-45	
b	IO	16	Write data setup	33		22	
c	M,IO	8	Write data setup (even)	7		-4	
d	M,IO	8	Write data setup (odd)	-45		-56	
12	M,IO	8/16	SA, SBHE* hold	53		42	
13a	M	16	Command deasserted	108		97	
b	M	8	Command deasserted	170		159	
c	IO	8/16	Command deasserted	170		159	
15a	M,IO	8/16	Read data hold	0		0	
b	M,IO		Write data hold	25		25	
16	M,IO	8/16	Read Command to SD disabled		30		30
17	M	16	ENDXFR* asserted from command		10		32
18	IO	8/16	IOCS16* asserted from SA		74		122
19	IO	8/16	IOCS16* hold from SA	0		0	
20a	M,IO	16	IOCHRDY valid from command asserted		70		159
b	M,IO	8	IOCHRDY valid from command asserted		373		462
21	M,IO	8/16	IOCHRDY deasserted pulse width	125	15600	125	15611
22	M,IO	8/16	Command hold from IOCHRDY	125			
23	M,IO	8/16	BALE asserted from command deasserted	46		35	
24	M,IO	8/16	Clock period (Tclk)	120	167	120	167
25a	M,IO	8/16	Data setup to IOCHRDY deasserted (8 bit even)		85		74
b	M,IO	8	Data setup to IOCHRDY deasserted (8 bit odd)		75		64
26a	M	16	LA hold to MEMx* active	41		30	
b	M	8	LA hold to MEMx* active	-21		-32	
28	M	16	ENDXFR* setup to SYSCLK falling edge	22			
29	M	16	ENDXFR* hold from SYSCLK falling edge	22			
30	M,IO	8/16	AEN deasserted to command asserted	111		100	
31	M,IO	8/16	AEN asserted from command deasserted	41		30	
32	M	8/16	AEN setup to BALE deasserted	111		100	
34	M,IO	8/16	SD disabled from read command asserted	0		0	
35	M,IO	8/16	IOCHRDY hold from command asserted	0		0	
36	M	16	LA setup to ENDXFR* asserted		180		158
37	M	16	SA setup to ENDXFR* asserted		83		61

Table 3.1. Memory and I/O Timing

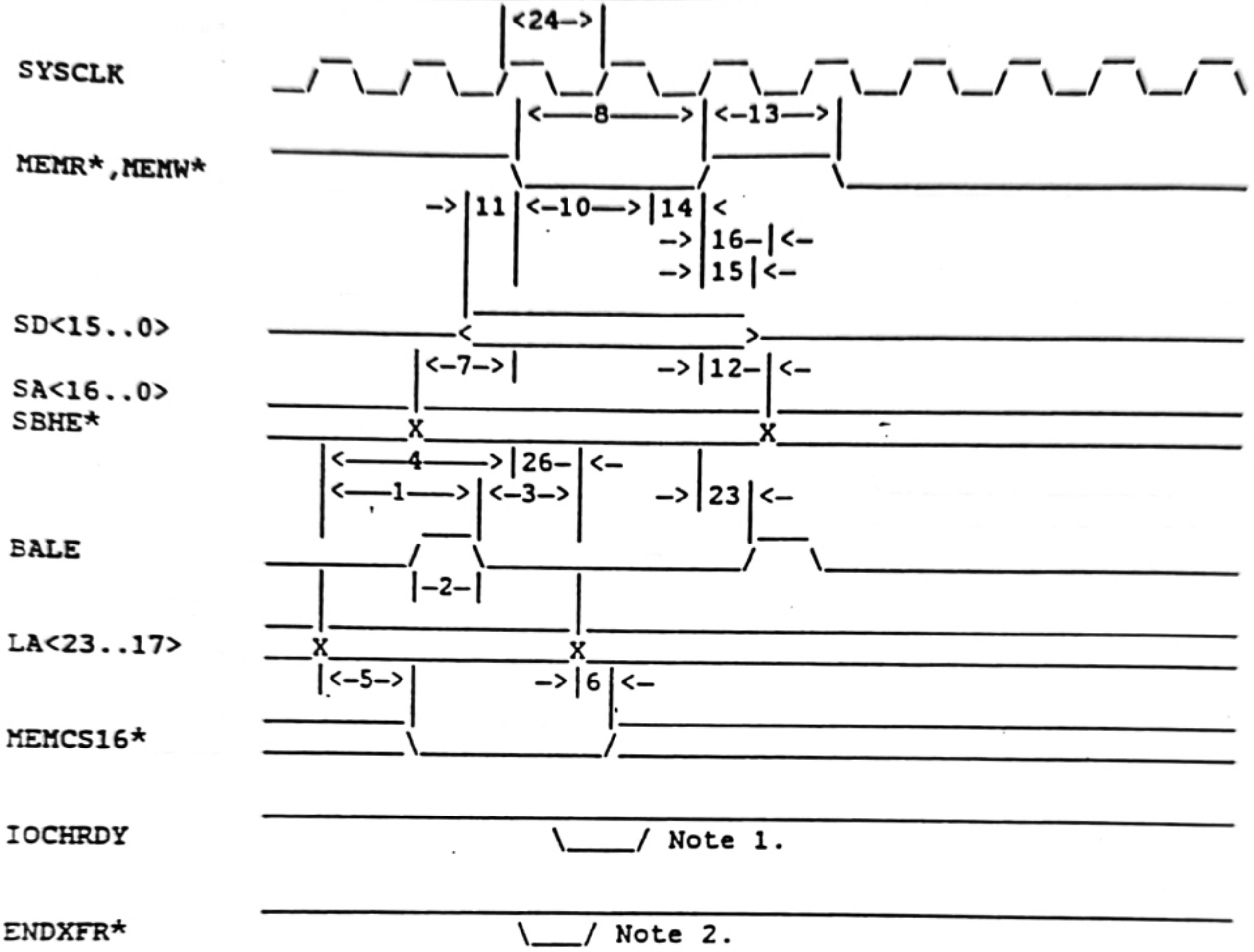

Figure 3.1. 16 bit Memory Timing:

Note:

1. IOCHRDY Timings apply if deasserted. See Figure 3.4 on page 3.7
2. ENDXFR* Timings apply if asserted. See Figure 3.5 on page 3.7

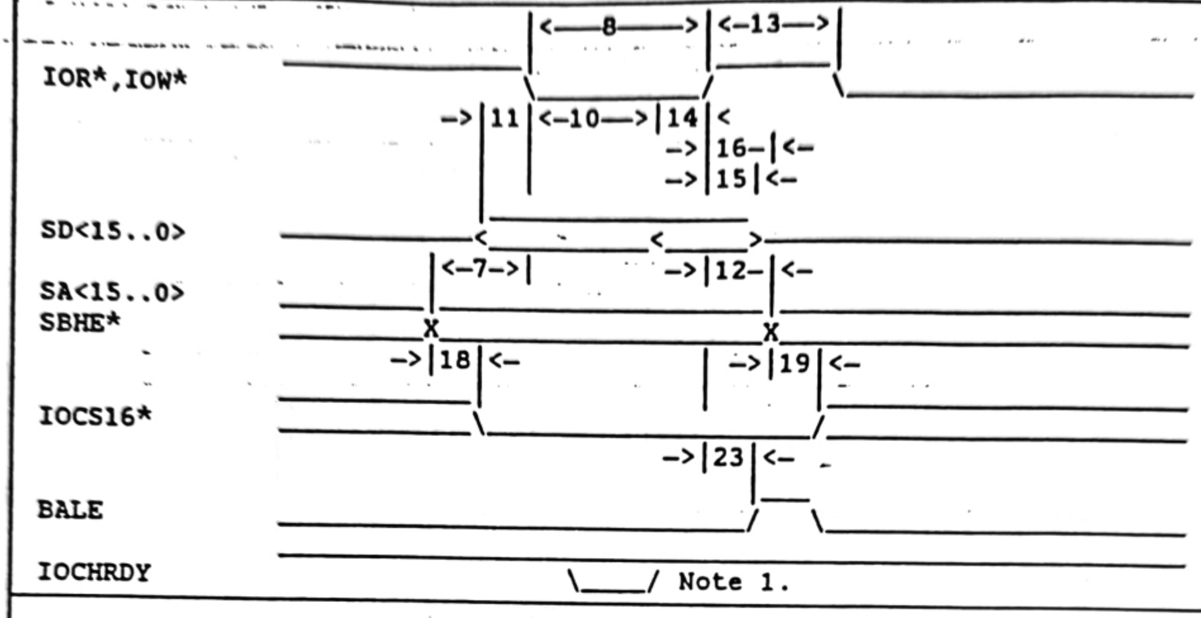

Figure 3.2. 16 bit I/O Timing:

Note:

1. IOCHRDY Timings apply if deasserted. See Figure 3.4 on page 3.7

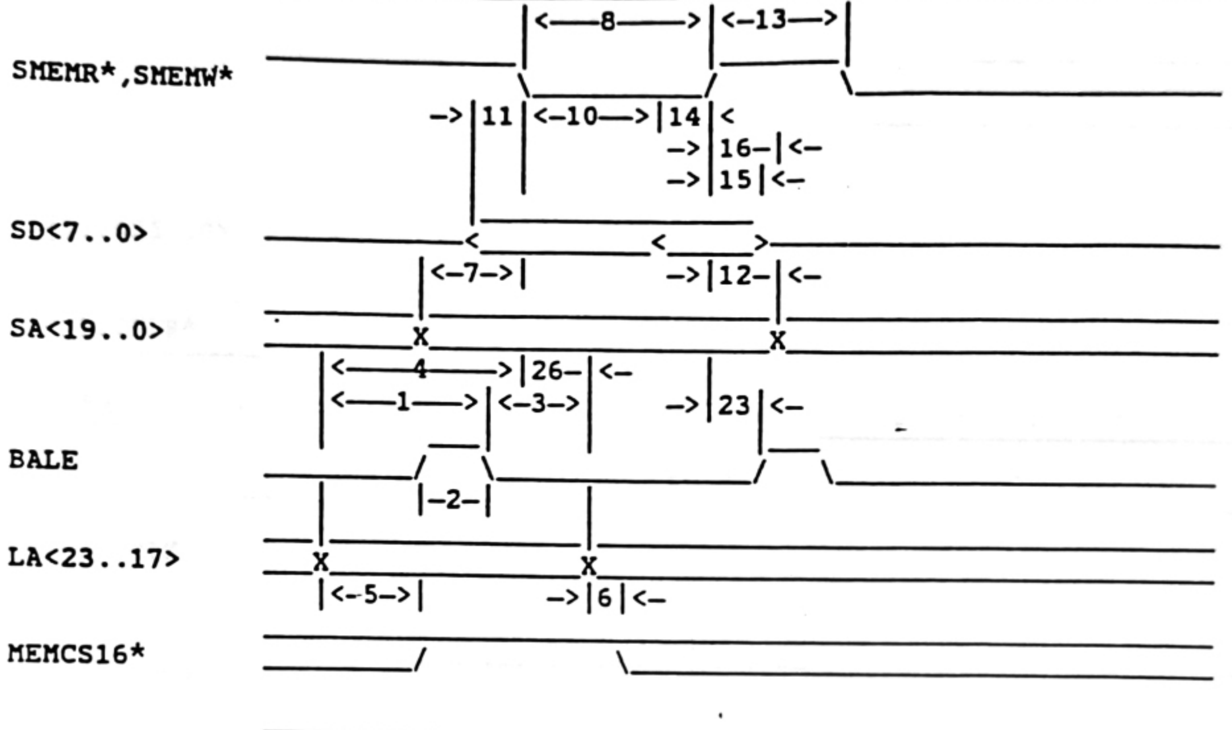

Figure 3.3. 8 bit Memory or I/O Timing:

Note:

1. `IOCHRDY` Timings apply if deasserted. See Figure 3.4 on page 3.7

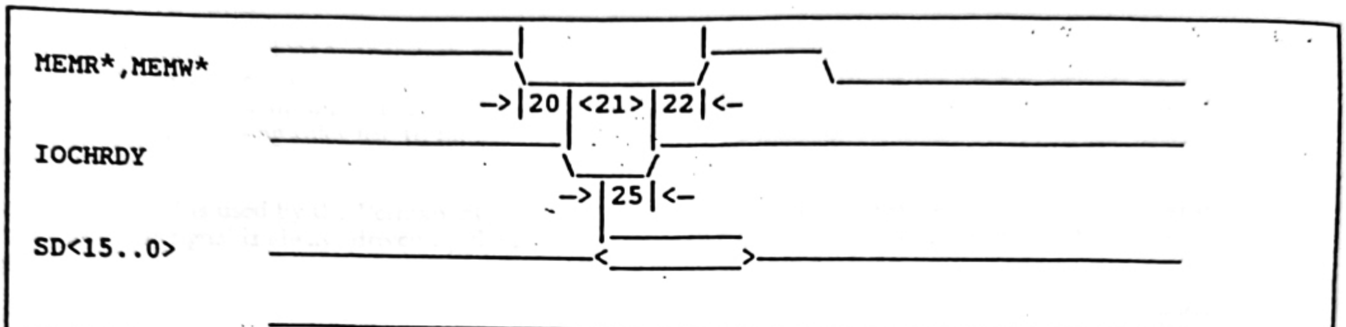

Figure 3.4. IOCHRDY Timing

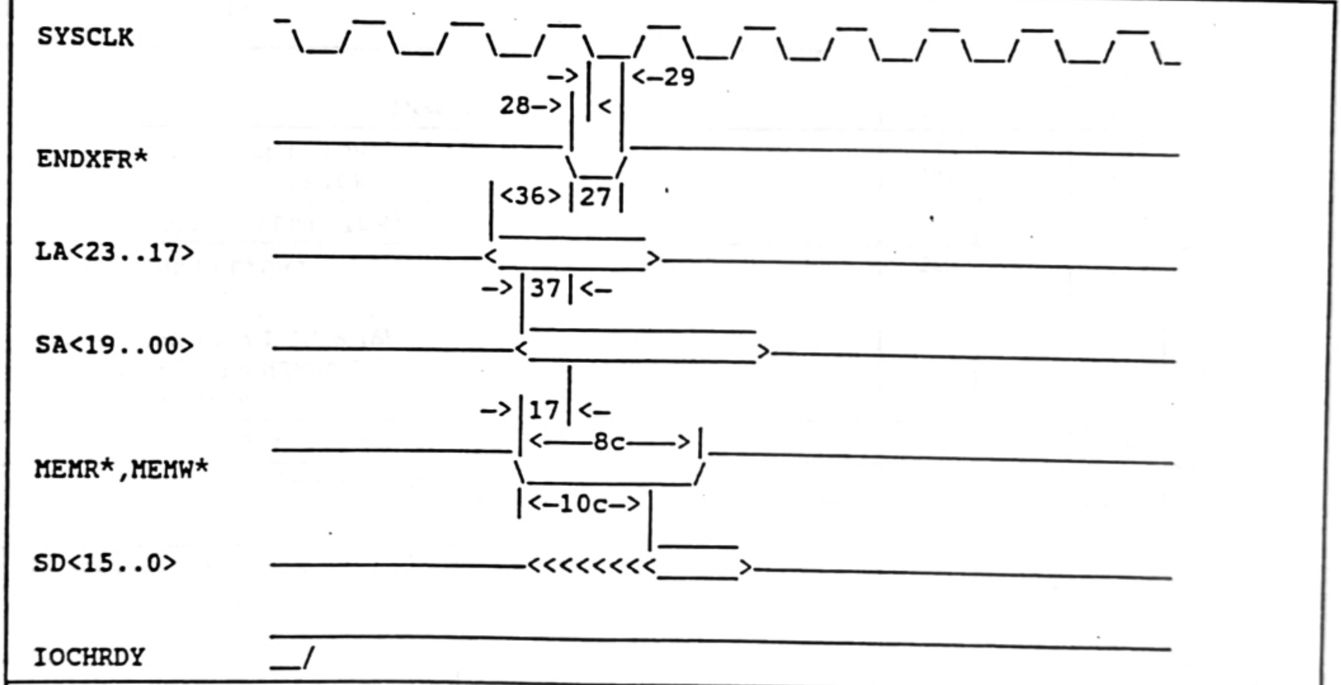

Figure 3.5. ENDXFR* Timing:

Note:

1. Assertion of ENDXFR* within the maximum time from command is only required for a 16 bit cycle with zero wait states, otherwise ENDXFR* may be asserted at any time during the cycle while command is asserted.

3.3 *DMA Operations*

Table 3.2 is a summary of DMA operation timing defined for DMA transfers illustrated in Figure 3.6 on page 3.9. Many of the parameters are used for several of the timing diagrams describing the various transfer operations on the bus. DMA transfer timing is determined by the width of the participating I/O and memory. If both are 16 bit devices then the timing rules for 16 bit operations are used. Under all other conditions, 8 bit timing rules should observed.

TC (Terminal Count) is used by the Permanent Master's DMA controller to indicate the last transfer in a particular block of data. This signal is always driven by the Permanent Master and may not be driven by an Alternate Master device.

Routing of data is described in Section 3.5.2, "Data Routing" for cases of 8 and 16 bit devices transferring data.

The DRQ*n* signal for a channel, once asserted, must remain asserted until the corresponding DACK**n* is received.

DMA devices that have requested the bus should not drive IOCHRDY to the inactive state, the request should not be generated unless data is available from the device.

BALE remains asserted throughout DMA and Alternate Master operations and therefore is not suitable for starting a memory access sequence.

ref	Description	Driver		Receiver	
		Min	Max	Min	Max
1a	DACK*n**, AEN setup to IOR*	76		65	
b	DACK*n**, AEN setup to IOW*	321		310	
2	Address setup to MEM*x**,IOW*	102		91	
3a	IOR* setup to MEMW*	246		234	
b	MEMR* setup to IOW*	0		0	
4a	Data access from IOR* 8/16b		220		242
b	Data access from MEMR* 16b		173		195
c	Data access from MEMR* 8b		332		337
5	Data setup to IOW* unasserted	164		142	
6	Read command hold from write cmd	50		39	
7	SBHE*, address hold	53		42	
8	Data hold from read command	11		0	
9a	IOCHRDY deasserted from 16b memory command		81		103
b	IOCHRDY deasserted from 8b memory command		384		406
10	TC hold from command unasserted	60		49	
11a	IOR* pulse width	797		786	
b	MEMR* pulse width	547		536	
12	IOW*, MEMW* width	500		489	
13a	DACK*n** hold from IOR*	114		103	
b	DACK*n** hold from IOW*	173		162	
c	AEN hold from cmd	41		30	
14	DREQ inactive from IO*x**		119		141
15	IOCHRDY low width	Tclk	15600	Tclk	15611
16	TC setup to command unasserted	511		500	

Table 3.2. DMA Timing

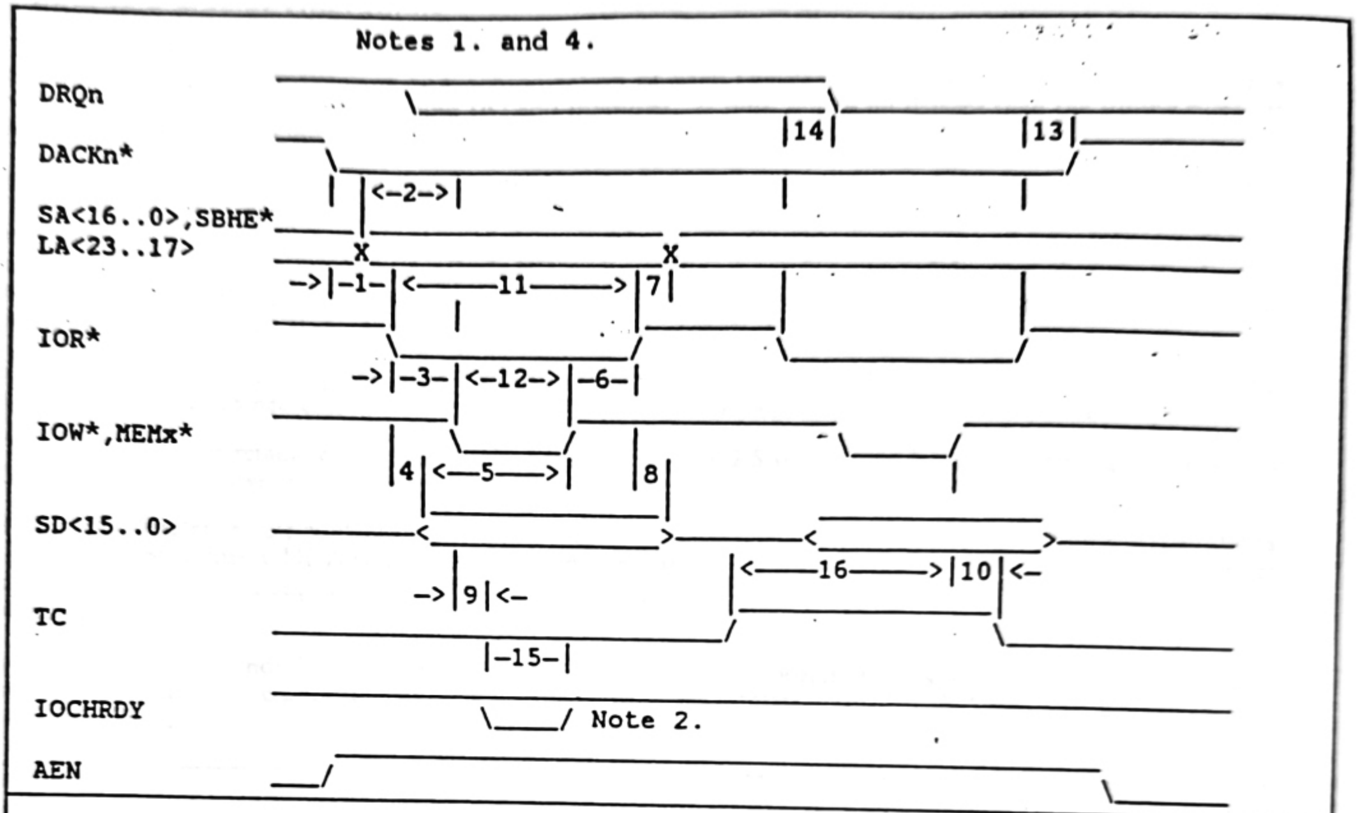

Figure 3.6. DMA Timing:

Note:

1. DRQ*n* may be deasserted anytime after DACK*n** during a block mode DMA transfer.
2. IOCHRDY may be deasserted to insert additional wait states. Additional bus wait states are added in units of two bus clocks.
3. The DMA controller activates TC during the last cycle of a DMA request.
4. DMA transfers may be broken up into multiple back-to-back cycles where the DMA controller removes DACK*n** and optionally releases the bus to allow higher priority cycles to occur. In this case DACK*n** will be temporarily deasserted even though DRQ*n* is still asserted.

3.4 *Alternate Master Operations*

This section describes data transfers between a Temporary Master and a target of different word width. Only the routing of data and not the sequencing or synchronization of such transfers is described. DMA transfer timing is determined by the width of the participating I/O and memory. If both are 16 bit devices then the timing rules for 16 bit operations are used. Under all other conditions, 8 bit timing rules are observed.

Timing for Alternate Master operations are identical to those specified for memory and I/O operations in Section 3.2, "Memory and I/O Operations" and in Figure 3.1 on page 3.4 through Figure 3.5 on page 3.7. The only exception is that `LA23..LA17` must be held valid for the entire cycle. Combined memory and I/O cycles (eg. DMA) are not available to a Temporary Master. Both I/O and memory operations are valid except that zero wait-state (`ENDXFR*`) timing is not supported because it would be difficult to achieve since the Alternate Master clock is either asynchronous or at least skewed from the Permanent Master clock.

Figure 3.7 depicts a *Bus Exchange* sequence which differentiates a Alternate Master cycle from others. Once the Temporary Master has gained control of the bus it may perform any combination of memory or I/O operations.

If a Temporary Master retains control of the bus for more than 2.5 microseconds certain existing bus adapters (DMA) may suffer data overrun conditions.

If a Temporary Master retains control of the bus for more than the refresh period (≈ 15μS), bus refresh operations must be performed to insure DRAM data validity. An alternate approach is to 'trigger' DMA or Alternate Master operations from the trailing edge of `REFRESH*` to ensure that the sequence completes and releases the bus before the refresh period occurs.

Some existing systems do not drive `MEMCS16*` correctly for the lower 256KB or 512KB of memory. It is advisable to provide for internal generation of that signal on an Alternate Master controller that needs to gain peak performance on the bus.

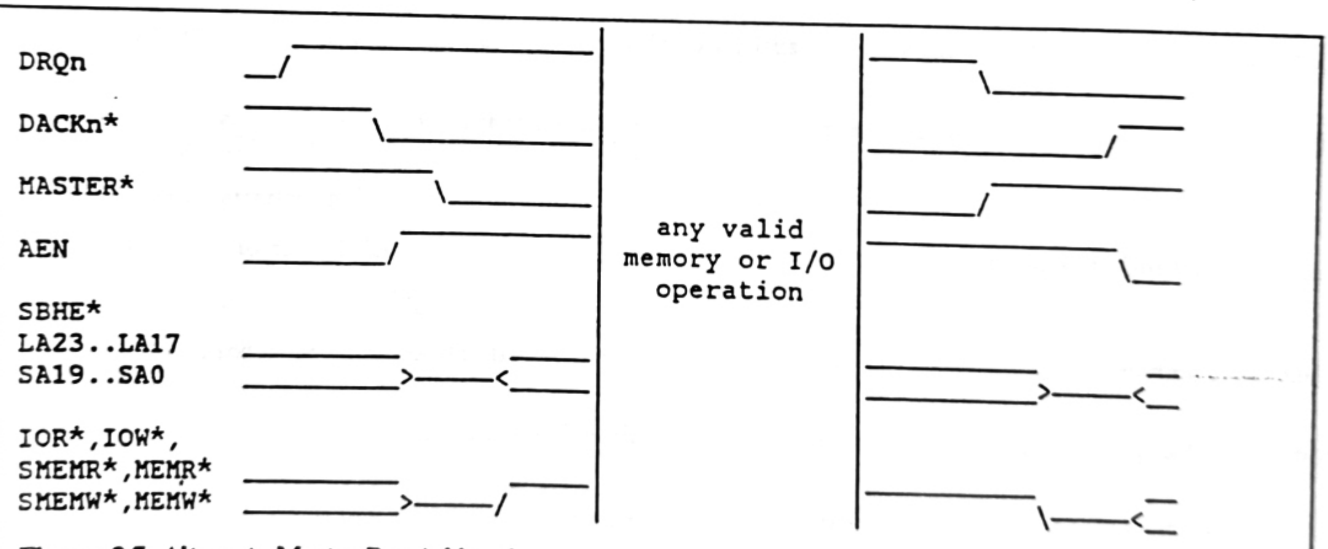

Figure 3.7. Alternate Master Bus Arbitration

.5 *Permanent Master*

There is one and only one device on a P996 bus that is described as the *Permanent Master* that's function is to

- Deal with generation of fixed timings signals
- Resolve bus allocation issues that by their nature require the involvement of a single centralized arbiter
- Facilitate the routing of data between devices of different widths.
- Detect and service interrupts.

In many systems, the Permanent Master is located on a *System Board* containing processors, memory and other key components of the system. In many systems, the Permanent Master also functions as a gateway between the P996 bus and other local memory or I/O buses that are tightly coupled to the processor. While this is a common arrangement, it is not the only one permitted by this specification.

The Permanent Master is a fixed device on the P996 bus. Its duties may not shift from board to board in the same way that alternate mastership may. Although more than one board may possess the logic needed to function as a Permanent Master, it is assumed that there is never any dynamic transfer of that function from board to board during normal bus operation.

The Permanent Master may also contain logic that allows it to function as an Alternate Master, or it may contain logic that allows it to function as the primary bus master device. In addition, it may function as a gateway to other such devices.

The Permanent Master must, by definition, be the widest device in any given bus system. Any devices narrower than the channel controller are attached in such a fashion that they are aligned in their least significant bits. That is: 8 bit devices are only allowed to be connected to `SD7..SD0`, 16 bit devices may only be connected to `SD15..SD0`, etc.

The Permanent Master must be capable of reading and writing data on all of the system's data lines in systems having more than 8 data lines. The Permanent Master has no data routing functions to perform in an 8 bit bus system since all devices are the same width.

The Permanent Master shall be capable of generating the following control signals:

SYSCLK: distributed as a reference clock to all Bus Adapters.

OSC: distributed as a reference to all Bus Adapters.

RESETDRV: broadcast to all Bus Adapters to reset them.

REFRESH*: distributed to indicate a refresh cycle to all Bus Adapters with DRAMs that do not perform local refresh.

BALE: indicates to a Bus Adapter that the **LA** lines are valid and may be latched on the falling edge. It is forced high during a DMA or Alternate Master operation.

AEN: when asserted indicates that the DMA device is driving the address lines.

TC: indicates to an I/O device involved in a DMA operation that this is the last transfer (DMA terminal count).

It should monitor the following signals:

SA0: which indicates when asserted that the current bus master device is transferring data starting at an odd byte address.

SBHE*: which indicates when asserted that the current bus master device is transferring data in or out on `SD15..SD8`.

MEMR*, MEMW*, IOR*, IOW*: all must be monitored to detect the direction and timing of transfers.

MEMCS16*, IOCS16*: are monitored to detect that the destination device addressed has 16 bit transfer capabilities of its own.

IRQ3..IRQ7, IRQ9..IRQ12, IRQ14..IRQ15: are monitored to detect interrupt conditions.

AEN, DRQ0..DRQ7, DACK0*..DACK7*: must all be monitored to track bus-to-bus transfers by "traditional" DMA devices. It is assumed that some information is conveyed by the allocation of these lines about the nature of the bus master involved in the transfer, and the Permanent Master is aware of this information. Systems supporting 8 bit devices assign channels 0-3 only to 8 bit devices and channels 4-7 only to 16 bit devices.

MASTER*: which indicates that the bus is in use by an Alternate Master device.

It may also generate or monitor signals for other purposes not related to data routing.

3.5.1 Initiator and Target Transfer Width Determination

The Permanent Master is the sole device with responsibility for output of data to the system data bus lines `SD15..SD0` from devices that require multiplexing services to adjust the routing of data between devices of different width. Ordinarily, this data is a copy of data currently being placed on another group of system data lines.

The Permanent Master monitors the bus signals generated by the Current Master in order to decide when and in which direction to multiplex data based on the initiator and target transfer widths.

It determines the width of the initiator by examining `SBHE*`. If the master is a 16 bit master doing a transfer to an odd byte address, this signal will be asserted. If it is not asserted, the initiator is either not a 16 bit master, or does not require multiplexing since it is transferring only low byte data.

The Permanent Master determines the width of the target in by examining `MEMCS16*` and `IOCS16*`. If none of these signals are asserted, the target is assumed to be an 8 bit device; if either of them is asserted, then the target width is 16 bits.

3.5.2 Data Routing

For transfers between 8 and 16 bit devices, the data transfer routing and those requiring crossover transfers performed by the Permanent Master are shown in Table 3.3.

Initiator		Operation	Target		`IOR*`	`IOW*`	`MEMR*`	`MEMW*`	`IOCS16*`	`MEMCS16*`	Normal Transfer	Crossover Transfer
PM, TM	16b	Write (→)	Mem	16b	1	1	1	0	X	0	HL→HL	
PM, TM	16b	Write (→)	Mem	8b	1	1	1	0	X	1	L→L	H→L
PM, TM	16b	Write (→)	I/O	16b	1	0	1	1	0	X	HL→HL	
PM, TM	16b	Write (→)	I/O	8b	1	0	1	1	1	X	L→L	H→L
PM, TM	16b	Read (←)	Mem	16b	1	1	0	1	X	0	HL←HL	
PM, TM	16b	Read (←)	Mem	8b	1	1	0	1	X	1	L←L	H←L
PM, TM	16b	Read (←)	I/O	16b	0	1	1	1	0	X	HL←HL	
PM, TM	16b	Read (←)	I/O	8b	0	1	1	1	1	X	L←L	H←L
DMA	16b	Write (→)	Mem	16b	0	1	1	0	X	0	HL→HL	
DMA	16b	Write (→)	Mem	8b	0	1	1	0	X	1	Illegal	
DMA	8b	Write (→)	Mem	16b	0	1	1	0	X	0	L→L	L→H
DMA	8b	Write (→)	Mem	8b	0	1	1	0	X	1	L→L	
DMA	16b	Read (←)	Mem	16b	1	0	0	1	X	0	HL←HL	
DMA	16b	Read (←)	Mem	8b	1	0	0	1	X	1	Illegal	
DMA	8b	Read (←)	Mem	16b	1	0	0	1	X	0	L←L	L←H
DMA	8b	Read (←)	Mem	8b	1	0	0	1	X	1	L←L	

Table 3.3. Data Transfer Routing Requirements

Note:

In the Initiator column, PM and TM are abbreviations for Permanent Master and Temporary Master, respectively.

2. H and L indicate the high or low byte transfer respectively, HL indicates that both high and low bytes of a word are transferred simultaneously. A H or L on the left side of a an arrow corresponds to the initiator, while a H or L on the right side of a an arrow corresponds to the target. The arrow indicates direction of transfer.

3. A target responding as an 8 bit device must not drive the high byte (SD15..SD8) of the bus to avoid interference with the crossover logic.

While the above data routing ensures that data appears correctly justified when it is transferred, a great deal of additional logic is needed to allow transparent transfers between devices of different widths since multiple transfers must be generated by the current bus master to move data from a wide device to a narrow one, and data from narrow devices must be retained and merged from several transfers when it is coming from a narrower device.

3.6 *Refresh*

A REFRESH* provides sequencing for refresh of dynamic memory residing on the P996 bus. Use of the REFRESH* line is optional by the bus adapter, however, generation of it by the Permanent Master is required. A Temporary Master other than the Permanent Master must initiate refresh cycles by asserting REFRESH* if it retains control of the bus for longer than 15 µS. The sequence required to generate refresh cycles is:

1. If the Permanent Master has control of the bus, it first asserts BALE at the start of a refresh operation. If an Alternate Master or Temporary Master has control of the bus, the Permanent Master will already be asserting BALE.
2. An Alternate Master must tri-state ins address and control drivers before asserting REFRESH*.
3. The Current Master asserts REFRESH* to begin the refresh operation. The Permanent Master will detect the assertion of REFRESH* and sequence a memory refresh operation by asserting SA7..SA0, SMEMR* and MEMR*. The values of SA19..SA8> and LA23..LA17 are undefined during the refresh operation. They may be driven or undriven (tri-stated).
4. The Current Master assert REFRESH* until after the deassertion of MEMR* so that the slave memory boards can differentiate between a refresh operation and a memory read operation.
5. The Permanent Master increments the refresh address at the deassertion of REFRESH*.
6. If the Current Master is also the Permanent Master, it deasserts BALE.

Refresh must be performed at a rate at least 256 operations every 4mS.

ref	Description	Driver		Receiver	
		Min	Max	Min	Max
1	MEMR* pulse width	214		203	
2	SA<07..0> setup to MEMR*	81		70	
3	SA<07..0> hold from MEMR*	36		25	
4	IOCHRDY deasserted from MEMR*		81		159
5	MEMR* deasserted from IOCHRDY	125		125	
6	REFRESH* setup to MEMR*	125		114	
7	REFRESH* hold from MEMR* Note 1.	31	250	20	239
8	SA<11..0>, MEMR* tri-state from MEMR* high		Tclk		
9	IOCHRDY width	Tclk		Tclk	
10	AM ownership delay Note 2.	2*Tclk		2*Tclk	
11	AEN asserted to MEMR* active	11		0	
12	AEN hold to MEMR* inactive	11		0	
13	REFRESH* asserted to SA<07..0> valid	11		0	
14	REFRESH* hold from SA<07..0> valid	11		0	
15	Address and Control disabled to REFRESH* asserted	0		0	

Table 3.4. Refresh Cycle Timing:

Note:

1. The Temporary Master may exceed the maximum REFRESH* hold time in order to conduct another refresh operation.
2. The Temporary Master, if the Current Master must tri-state the address and command signals prior to driving REFRESH* = L.

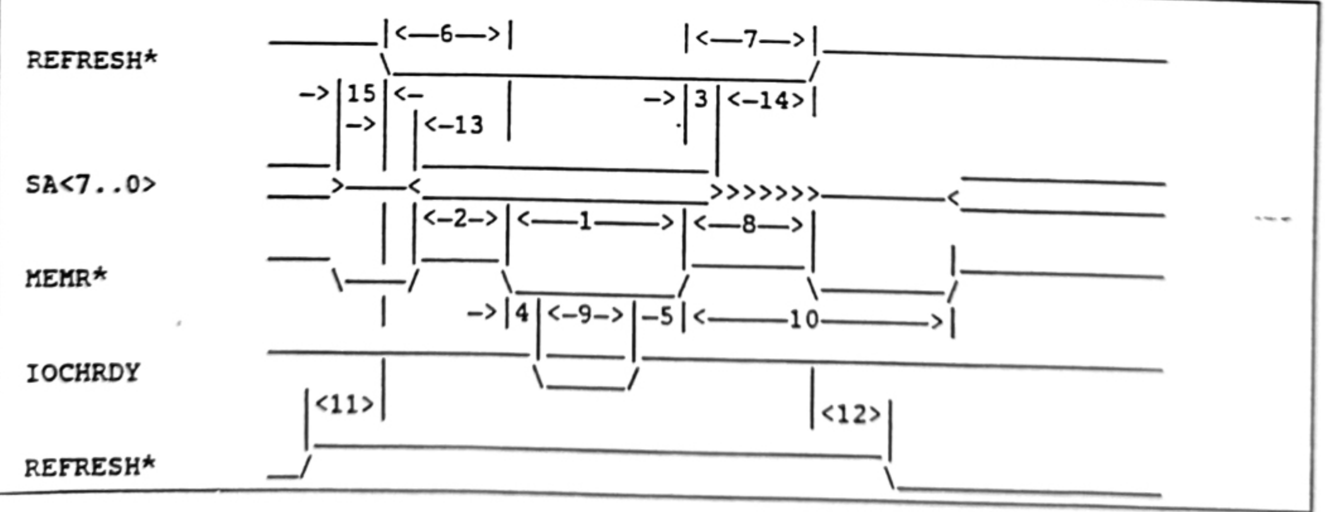

Figure 3.8. Refresh Timing

4. Interrupt Operations

The interrupt request lines, `IRQ3..IRQ7`, `IRQ9..IRQ12`, `IRQ14..IRQ15` signal the Permanent Master that a adapter requires service. The processor on the Permanent Master acknowledges the interrupt and takes the required action with the appropriate interrupt service routine.

4.1 Non-shared Interrupts

Non-shared interrupts allow only one adapter to use an interrupt request line at the same time. Initially the adapter currently using IRQ*n* drives it to a LOW state. The adapter generates an interrupt by either driving it to an HIGH state if using a tri-state driver or by releasing the the active pulldown if using a open-collector driver allowing it to be pulled to a HIGH state by the resistive pull-up. IRQ*n* must remain at a HIGH state until the interrupt is acknowledged.

After the interrupt is acknowledged, the interrupt service routine must cause the adapter to return IRQ*n* to an LOW state.

When the adapter no longer requires interrupt service, it should remove its active drive (tri-state or open-collector) of IRQ*n* so that it may be used by another adapter.

4.2 Shared Interrupts

Shared interrupts allow more than one adapter use a common interrupt request line. A requestor must have an interrupt status latch that is set before the an interrupt is initiated. The processor starts an interrupt sequence on the rising edge of a negative pulse (125 to 1000 nSecs) of the interrupt request line. The interrupt status latch must be reset (and the interrupt level re-enabled) by the interrupt service routine. The interrupt line should be driven with an open-collector driver or or tri-state equivalent (e.g., LS125 with input connected to +5V, enabled when interrupt is to be asserted).

5. Bus Arbitration

5.1 *Introduction*

This section specifies bus arbitration operations where bus ownership is transferred between the Permanent Master and an Alternate Master.

5.2 *Arbitration Timing Specification*

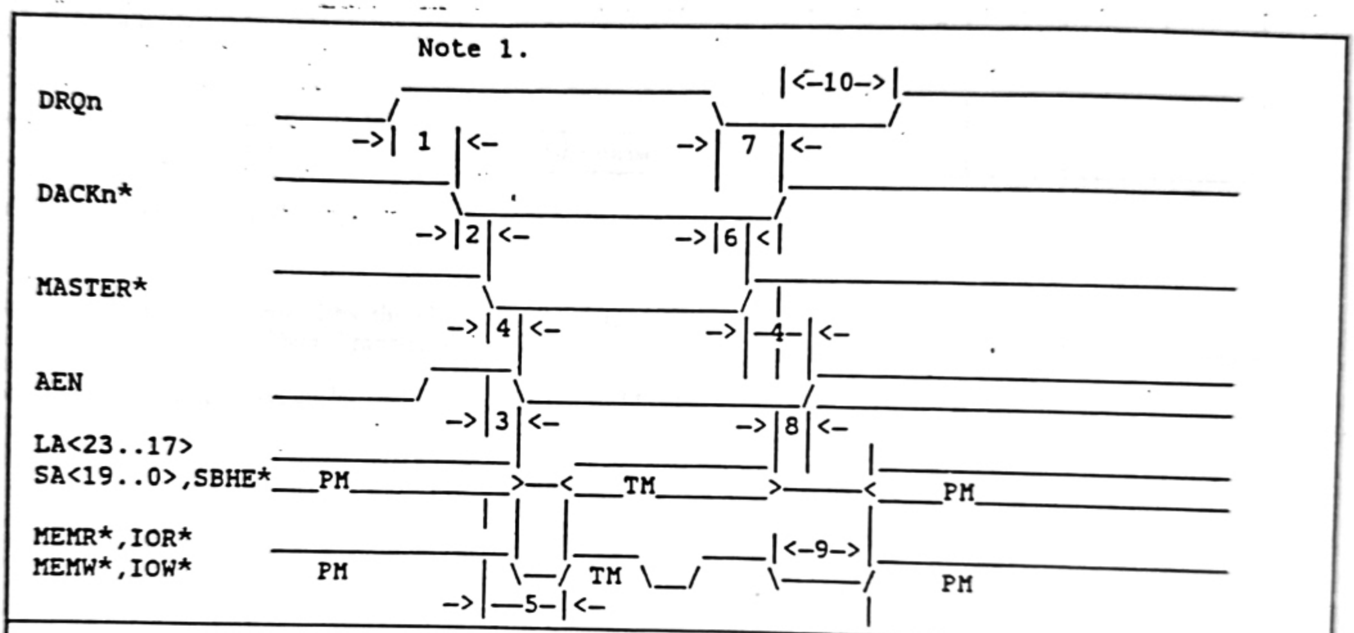

Figure 5.1. Bus Arbitration Timing:

Note:

1. Refer to Figure 3.6 on page 3.9 for operations run by the Temporary Master.
2. PM and TM are abbreviations for Permanent Master and Temporary Master.

ref	Description	Driver		Receiver	
		Min	Max	Min	Max
1	DRQn active to DACKn* active, Note 1.				
2	DACKn*to MASTER* delay	0			
3	Permanent Master tri-states bus signals	0	49		60
4	AEN delay from MASTER*	0	49		71
5	Alternate Master drives address and data signals, Note 2.		125		
6	MASTER* delay from DRQn inactive		100		
7	DACKn* inactive from DRQn inactive, Note 3.	375		375	
8	Alternate Master tri-states bus signals	0			
9	Permanent Master drives bus signals	49		60	
10	DRQn inactive hold from DACKn*	0			
11	Alternate Master inactive from last command unasserted.	60			

Table 5.1. Bus Arbitration Timing

Note:

1. The exact timing is determined by the DMA controller.
2. Refer to Section 2.5.1, "Data Transfer Operations" for the timing of operations executed by the Alternate Master.
3. The Alternate Master driving the command lines should adhere to the command to address and data setup times specified in Section 2.5.1, "Data Transfer Operations".

6. Bus Initialization

6.1 *Introduction*

This section defines the timing of the initialization sequence after reset and the initial state of signals on the bus.

6.2 *Initialization Timing*

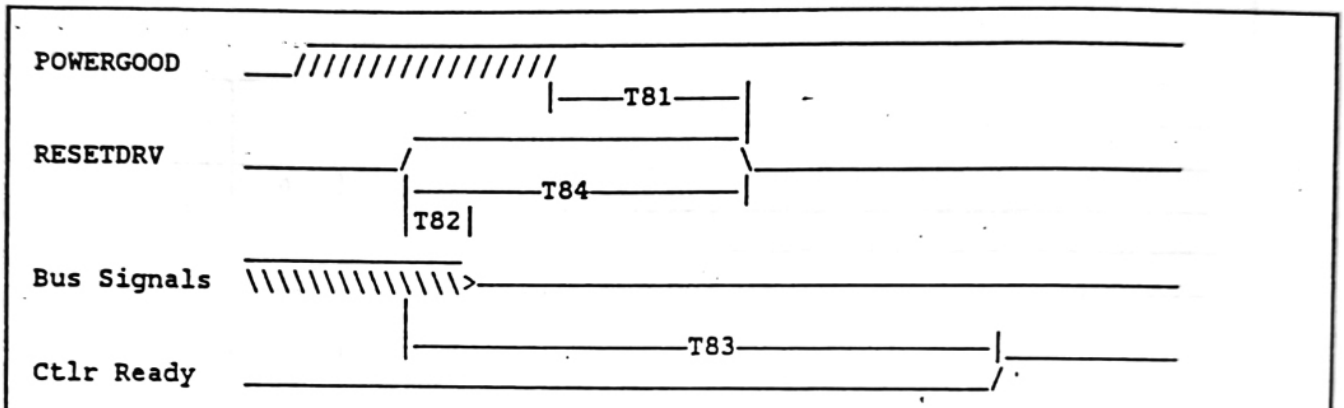

Figure 6.1. Initialization Timing

ref	min	max	Type	Size	Description
T81	1mS				POWERGOOD to RESETDRV deasserted
T82	0	500nS			RESETDRV asserted to bus signals inactive
T83	0	1mS			RESETDRV asserted to bus adapters ready
T84	9*Tclk				RESETDRV pulse width

Table 6.1. Initialization Timing Summary: POWERGOOD is a signal usually generated by the local power supply indicating that the power supply voltage levels are stable.

T83 is the time that bus adapters have to initialize themselves. After this time it should be possible to at least query the adapter and have it return "not ready". It does not include time for an attached peripheral, e.g., a disk drive, to become "ready".

6.3 *Initial State*

The initial state of signals on the P996 bus after **RESETDRV** goes inactive is:

Signals	Level	State	Comments
Address Lines			
`LA23..LA17`	x	inactive	
`SA19..SA0`	x	inactive	
`SBHE*`	1	inactive	
Data Lines			
`SD15..SA0`	x	inactive	
Utilities/Controls			
`SYSCLK`		active	
`OSC`		active	
`RESETDRV`	0	inactive	
Utilities/Commands			
`BALE`	0	inactive	
`IOR*`, `IOW*`, `SMEMR*`, `SMEMW*`, `MEMR*`, `MEMW*`	1	inactive	
Utilities/Transfer Response			
`IOCS16*`, `MEMCS16*`	1	inactive	
`ENDXFR*`	1	inactive	
`IOCHCHK*`	1	inactive	
`IOCHRDY`	1	inactive	
Utilities/Interrupts			

`IRQ3..IRQ7`
`IRQ9..IRQ12`
`IRQ14..IRQ15`
	1	asserted	Pulled up by the Permanent Master. Interrupts should be masked in the interrupt controller (8259 or equivalent).

Bus Arbitration/DMA			
`DRQ0..DRQ3`, `DRQ5..DRQ7`	0	inactive	
`DACK0*..DACK3*`, `DACK5*..DACK7*`	1	inactive	
`AEN`	0	inactive	
`REFRESH*`	1	inactive	
`TC`	0	inactive	
Bus Arbitration/Arbitration Control			
`MASTER*`	1	inactive	

Table 6.2. Initial Signal State

7. Bus Error

A bus operation error is signalled with `IOCHCHK*`. This must be asserted for the period specified in Table 7.1 to guarantee that it will be sampled. It is cleared by the next memory reference with no error, e.g., a good DRAM access or read from the ROM.

7.1 *Timing*

ref	min	max	Type	Size	Description
T71	Tclk				`IOCHCHK*` pulse width

Table 7.1. Initialization Timing Summary

8. Board Specifications

8.1 *Introduction*

This section specifies requirements and restrictions for add-in boards that will be used on the P996 bus. These should be met to guarantee compatibility and reliable operation.

8.2 *Electrical Characteristics*

8.2.1 Power/Voltage Requirements

These specifications are measured at the connector over the full temperature range.

Supply	Min	Max	Current	Comments
+12V	+11.4V	+12.6V	1.0A	±5%
+5V	+4.875V	+5.25V	4.5A	+5%, -2.5%
-5V	-5.25V	-4.75V	0.2A	±5%
-12V	-12.6V	-11.4V	0.3A	±5%
0V	0.0V	0.0V	5.5A	

Table 8.1. Power Supply Voltage/Current Specifications

8.2.2 Bus Receiving and Driving Requirements

DC receiver input and driver output levels and measurement conditions are tabulated in Table 8.2. The receiver input characteristics can be satisfied using LS or ALS TTL or their equivalents. All measurements made from 0-70°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units	Comments
V*ih*	Input high	I*i* = I*ih*	2.0			V	
V*il*	Input low	I*i* = I*il*			0.8	V	
V*t*	Input Threshold			1.5		V	
I*ih*	Input high	V*i* = 2.0V			20	µA	Each receiver
I*il*	Input low	V*i* = 0.8V			-200	µA	Each receiver

Table 8.2. Receiver Input DC Parameters

Note: Current flow is defined as positive if it enters a device and negative if it leaves the device.

There are three classes of drivers specified by P996 that are described in Table 8.4 on page 8.3. These are combinations of tri-state, open collector, and totem-pole lines with or without pullup/termination resistors.

V*oh*	Output high	I*o* = I*oh*	2.4			V	TP, enabled TS driver
V*ol*	Output low	I*o* = I*ol*			0.5	V	TP, enabled TS driver
I*oh*	Output high leakage	V*o* = V*cc*			200	µA	OC driver
I*oh*	Output high	V*o* = 2.4V				*m*A	Table 8.4 on page 8.3
I*ol*	Output low	V*o* = 0.5V				*m*A	Table 8.4 on page 8.3

Table 8.3. Driver Output DC Parameters

8.2.3 Stub Length

The signal stub length is defined as the length of the longest trace from the connector pin to the drivers or receivers of this board. The maximum stub length is 2.5 inches.

8.2.4 Loading

Each adapter board shall present no more than the equivalent of two (LS or ALS equivalent) receiver input loads and a maximum capacitive load of 15pF on each signal line. The capacitive load specification includes driver output capacitance.

Certain lines TC and DACKx* are driven from the Permanent Master to the Bus Adapters with reduced DC current capability and are permitted only a single receiver input load on each Bus Adapter.

8.2.5 Min/Max Rise and Fall Times

The minimum output rise and fall times of drivers measured at the adapter board is 3ηS. This can be achieved using LS or ALS compatible drivers, the use of F or AS compatible drivers is not recommended.

Driver AC current capability should be carefully chosen to meet these requirements. Use of devices with faster switching characteristics will increase the bus settling times and will increase rather than decrease the delay to a stable output.

8.3 *Mechanical Characteristics*

Skirts, the area below the board adjacent to the edge connector fingers, are not recommended to prevent interference with components on the system board.

8.3.1 Board Outline, 8 bit Form Factor Printed Circuit Boards

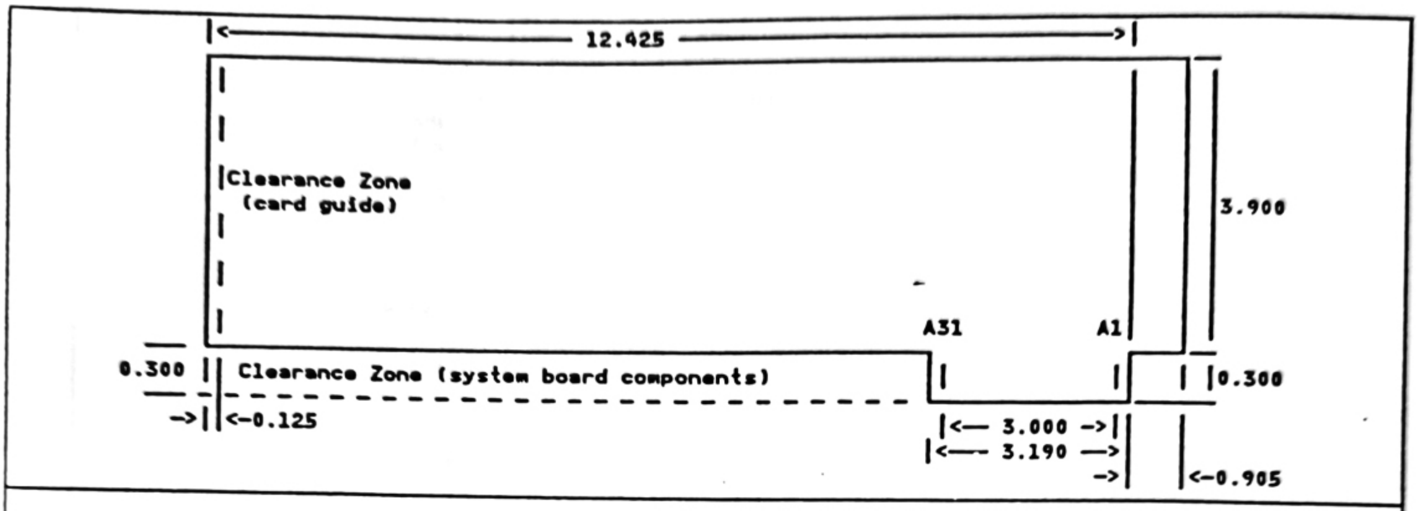

Figure 8.1. 8 bit Form Factor Board Outline Drawings: Notes:

1. All units in inches.
2. Dimensions for connector finger spacing are center-line to center-line.
3. 0.905 dimension may be smaller depending on bracket mounting method used.
4. Card edge fingers are centered in the connector tabs.

No skirts are permitted on 8 bit form factor boards in the area where the 16 bit (C/D) connector would go on a 16 bit form factor board.

	Signal	Pin	Pin	Signal
P1	0V	B01	A01	IOCHCHK*
	RESETDRV	B02	A02	SD7
	+5V	B03	A03	SD6
	IRQ9	B04	A04	SD5
	-5	B05	A05	SD4
	DRQ2	B06	A06	SD3
	-12V	B07	A07	SD2
	ENDXFR*	B08	A08	SD1
	+12V	B09	A09	SD0
	0V	B10	A10	IOCHRDY
	SMEMW*	B11	A11	AEN
	SMEMR*	B12	A12	SA19
	IOW*	B13	A13	SA18
	IOR*	B14	A14	SA17
	DACK3*	B15	A15	SA16
	DRQ3	B16	A16	SA15
	DACK1*	B17	A17	SA14
	DRQ1	B18	A18	SA13
	REFRESH*	B19	A19	SA12
	SYSCLK	B20	A20	SA11
	IRQ7	B21	A21	SA10
	IRQ6	B22	A22	SA9
	IRQ5	B23	A23	SA8
	IRQ4	B24	A24	SA7
	IRQ3	B25	A25	SA6
	DACK2*	B26	A26	SA5
	TC	B27	A27	SA4
	BALE	B28	A28	SA3
	+5V	B29	A29	SA2
	OSC	B30	A30	SA1
	0V	B31	A31	SA0

Bracket End ↑

← Add-in Board Component Side

	Signal	Pin	Pin	Signal
P2	MEMCS16*	D01	C01	SBHE*
	IOCS16*	D02	C02	LA23
	IRQ10	D03	C03	LA22
	IRQ11	D04	C04	LA21
	IRQ12	D05	C05	LA20
	IRQ15	D06	C06	LA19
	IRQ14	D07	C07	LA18
	DACK0*	D08	C08	LA17
	DRQ0	D09	C09	MEMR*
	DACK5*	D10	C10	MEMW*
	DRQ5	D11	C11	SD8
	DACK6*	D12	C12	SD9
	DRQ6	D13	C13	SD10
	DACK7*	D14	C14	SD11
	DRQ7	D15	C15	SD12
	+5V	D16	C16	SD13
	MASTER*	D17	C17	SD14
	0V	D18	C18	SD15

Figure 9.1. P996 Connector Pin Assignments (System Board, Top View): The bottom of the figure is the front (bezel side) of the system.

Signal	Pin	Pin	Signal
IOCHCHK*	A01	B01	0V
SD7	A02	B02	RESETDRV
SD6	A03	B03	+5V
SD5	A04	B04	IRQ9
SD4	A05	B05	-5
SD3	A06	B06	DRQ2
SD2	A07	B07	-12V
SD1	A08	B08	ENDXFR*
SD0	A09	B09	+12V
IOCHRDY	A10	B10	0V
AEN	A11	B11	SMEMW*
SA19	A12	B12	SMEMR*
SA18	A13	B13	IOW*
SA17	A14	B14	IOR*
SA16	A15	B15	DACK3*
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1*
SA13	A18	B18	DRQ1
SA12	A19	B19	REFRESH*
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2*
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	+5V
SA1	A30	B30	OSC
SA0	A31	B31	0V

Bracket End ↑

← **Add-in Board Solder Side**

SBHE*	C01	D01	MEMCS16*
LA23	C02	D02	IOCS16*
LA22	C03	D03	IRQ10
LA21	C04	D04	IRQ11
LA20	C05	D05	IRQ12
LA19	C06	D06	IRQ15
LA18	C07	D07	IRQ14
LA17	C08	D08	DACK0*
MEMR*	C09	D09	DRQ0
MEMW*	C10	D10	DACK5*
SD8	C11	D11	DRQ5
SD9	C12	D12	DACK6*
SD10	C13	D13	DRQ6
SD11	C14	D14	DACK7*
SD12	C15	D15	DRQ7
SD13	C16	D16	+5V
SD14	C17	D17	MASTER*
SD15	C18	D18	0V

Figure 9.2. P996 Connector Pin Assignments (System Board, Bottom View): The bottom of the figure is the front (bezel side) of the system.